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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. KM1-003	SERIAL NO.		
<b>LIST OF ART CITED BY APPLICANT</b> (Use several sheets if necessary)				APPLICANT Keiji Iono et al.			
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TT	AR		Shallow Trench Isolation Characteristics with High-Density-Plasma Chemical Vapor Deposition Gap-Fill Oxide for Deep-Submicron CMOS Technologies, Seung-Ho Lee et al., Jpn. J. Appl. Phys. Vol. 37 (1998), pp. 1222-1227.				
TT	AS		Impact of Shallow Trench Isolation on Reliability of Buried- and Surface-Chanel sub- $\mu$ m PFET, William Tonti et al., 1995 IEEE. pp. 24-29.				
TT	AT		Subbreakdown Drain Leakage Current in MOSFET, J. Chen et al., 1987 IEEE, pp.515-517.				
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II	AR		Shallow Trench Isolation for advanced ULSI CMOS Technologies, M. Nandakumar et al, Silicon Technology Development,				
			Kilby Center, Texas Instruments, Undated, 4 pages.				
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EXAMINER <i>Wen KML</i>				DATE CONSIDERED <i>01-23-03</i>			
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